Review of the DFEA2 prototype board – PRR – 13 January 2005
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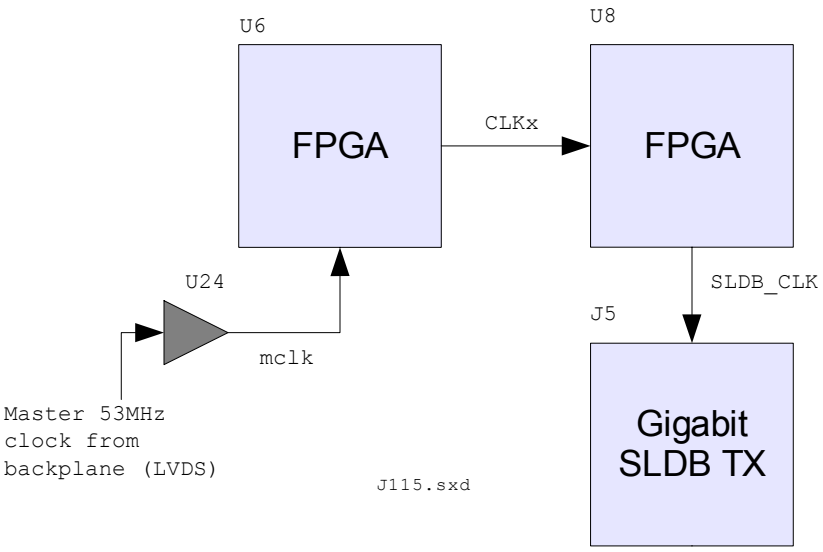
Clock Distribution Concerns

It appears that the Master 53MHz clock is run through several FPGAs like this:



What mechanism is in place to insure that excessive jitter and skew does not accumulate on this clock net as it passes through two layers of IBUFs, FPGA internal routing, DLLs, and OBUFS?

The AMCC device (S2042) used on the SLDB transmitter requires clock jitter less than +/-100 ppm.

Power Supply

If there is noise on the +48V and +48VRTN lines it will be capacitive coupled into the experiment ground via C241, C242, C240, and C243. This may cause problems with the sensitive analog electronics nearby. We recommend that these capacitors should not be stuffed.

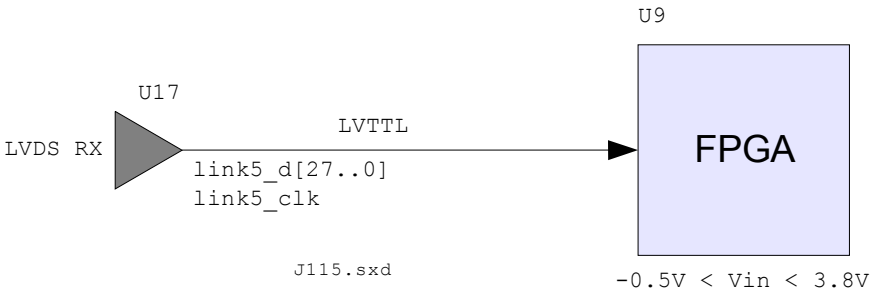
Input Link Bus Architecture

The DFEA scheme used external buffers to send a copies of the input link data directly to multiple FPGAs. The DFEA2 bus architecture requires the **up_front** and **down_front** FPGAs to receive and retransmit link data to the **up_back** and **down_back** FPGAs.

Please demonstrate that this additional latency penalty will not affect the overall L1 latency of the board and it will meet or exceed the DFEA latency performance as specified by the DFEA TDR [1].

Input Link Termination

There do not appear to be any external termination resistors between the LVDS receiver (SN65LVDS94) and the **up_front** and **down_front** FPGAs:



Fast rise and fall times on these LVTTL signals may damage the inputs on the FPGA inputs if not properly terminated. The LVDS RX datasheet shows a typical t_R of 3ns [2].

Xilinx Application Note XAPP659 [3] states that "the LVDCI_33 standard does not offer input termination"... if this is indeed the case how are these signals terminated?

References

1. DFEA TDR: http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs/tdr/dfea_tdr.pdf

2. TI Datasheet: http://focus.ti.com/docs/prod/folders/print/sn65lvds94.html

3. Xilinx XAPP659: http://www.xilinx.com/bvdocs/appnotes/xapp659.pdf